REMARKS

The examiner rejected claims 1-23 under 35 U.S.C. 102(b) as being anticipated by Chang et al US Patent 5,634,015.

Claims 1-23 as amended are distinct over Chang. Claim 1, as amended for instance, recites a method that includes... storing queue descriptors in a memory, determining which of the queue descriptors stored in the memory were most recently accessed according to a criterion, and storing the determined subset of queue descriptors in a cache in a processor's memory controller logic.

In Chang's system packets are stored in a packet memory, and "for each buffer in the packet memory (PM) there is one corresponding buffer table entry in the GAM local memory 30" (col. 17, lines 24-26). "In the GAM, packet buffers are linked together through the next buffer pointer in the BTR. Once a packet is stored in the PM, it will be treated as a unit by the GAM 18. To represent this unit, the GAM has one packet table entry (PTE) in its local memory for each existing packet in the PM" (emphasis added, col. 17, lines 60-63). Since the packet can be stored in multiple locations (buffers) within the packet memory, the GAM local memory 30 stores a buffer table entry for each buffer in the packet memory and GAM 18 stores an entry for each packet. Since Chang stores an entry for each packet, Chang does not describe or suggest "determining which of the queue descriptors stored in the memory were most recently accessed according to specific criteria, and storing the determined subset of queue descriptors in a cache in a processor's memory controller logic" as in the applicant's claim 1.

For at least the same reasons, applicant submits claim 1 should be allowed, applicant submits that dependent claims 2-8 should be allowed.

Claim 9 distinguishes by reciting a "memory controller logic that includes a cache to store a subset of the queue descriptors in the memory, the subset determined based on which of the queue descriptors stored in the memory were most recently accessed according to a criterion." Thus, based on these limitations claim 9 is patentable for reasons similar to claim 1.

For at least the same reasons, applicant submits claim 9 should be allowed, applicant submits that dependent claims 10-15 should be allowed.

Claim 16 as amended includes instructions causing a computer to "store queue descriptors in a memory, the queue descriptors each specifying a structure of a respective queue, determine which of the queue descriptors stored in the memory were most recently accessed according to a criterion, [and] store the determined a subset of queue descriptors in a cache in a processor's memory controller logic." Thus, based on these limitations claim 16 is patentable for reasons similar to claim 1.

For at least the same reasons, applicant submits claim 16 should be allowed, applicant submits that dependent claims 17-23 should be allowed.

The fact that the applicant has addressed certain comments of the examiner does not mean that the applicant concedes any other positions of the examiner. The fact that the applicant has asserted certain grounds for the patentability of a claim does not mean that there are not other good grounds for patentability of that claim or other claims.

Please apply any charges or credits to deposit account 06-1050, referencing Attorney Docket No. 10559-610001.

Respectfully submitted,
Attorneys for Intel Corporation,

Date: 2/24/04

Denis G. Maloney
Reg. No. 29,670

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

20811164.doc